ALHAD DAFTARDAR

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Education

UNIVERSITY OF MICHIGAN | Ann Arbor, MI *August 2020 –*
Doctor of Philosophy in ECE Expected Graduation, May 2025

GEORGIA INSTITUTE OF TECHNOLOGY | Atlanta, GA *August 2016 – May 2020*
BSEE, CS Minor (Intelligence Concentration), 4.00 GPA
Honors Program Graduate
Recipient of ECE Senior Scholar Award
Recipient of Batts and Brown Innovation Award ($4000 scholarship) – *via the Vertically Integrated Projects program*

Publications

P. Coppock, **A. Daftardar**, Z. Tolaymat, M. Yacoub, and V. Mooney, "Hardware Root-of-Trust Based Integrity for Shared Library Function Pointers in Embedded Systems," submitted to *Microprocessors and Microsystems* on 1 November 2019, **under review**.

G. Lopez, M. Foreman, **A. Daftardar**, P. Coppock, Z. Tolaymat and V. Mooney, "Hardware Root-of-Trust Based Integrity for Shared Library Function Pointers in Embedded Systems," *2019 8th Mediterranean Conference on Embedded Computing* (MECO'19), pp. 196-201, June 2019.

Work Experience

Systems & Technology Research | Boston, MA *May 2019 – August 2019*
Cyber Physical Systems Intern
Project Title: Software Defined Hardware (DARPA Initiative)

- Programming language design & development targeting accelerated hardware for computationally intensive algorithms (e.g. machine learning, graph search)
- Learned/self-taught MITCHELL language & implemented NLP algorithms to demonstrate MITCHELL's massive parallelism features
- Developed and demonstrated a full, proof-of-concept pipeline from algorithm implementation in MITCHELL, to compilation to low-level libraries [that I customized], to simulation onto hardware-accelerator simulators

Research Experience

Vertically Integrated Projects: Agile Communication Architectures | Atlanta, GA *August 2019 – May 2020*
Undergraduate Research Assistant, Blue Team Lead
Project Title: Automatic Modulation Classification on SDRs using ResNet Classifier

- Implementing machine learning models on Software Defined Radios for use in modulation classification
- Utilizing GNURadio software to create customized communication blocks containing both traditional DSP filters and customized code blocks embedded with ML algorithms (e.g. for predicting classification labels)
- Led Blue Team (Spring 2020) in the direct implementation of ML classifiers onto SDRs for signal classification in real-time

Vertically Integrated Projects: Secure Hardware | Atlanta, GA *August 2018 – May 2020*
Undergraduate Research Assistant, Senior Member
Project Title: Hardware Root-of-Trust Based Integrity for Shared Library Function Pointers in Embedded Systems

- Developed a secure hardware root-of-trust (RoT) to mitigate effects of malware attacks on the Global Offset Table (GOT)
- Implemented RoT in Verilog modules programmed onto Xilinx Zedboard with PetaLinux OS for software interface
- Wrote malware that overwrote GOT function pointers and succeeding in redirecting program flow in absence of RoT
- Demonstrated RoT storage/retrieval interface that eliminated program dependence on GOT and nullified malware effects
- Learnt operating system concepts (shared libraries, dynamic linking, GOT-PLT interaction, ELF hierarchies)
- Published conference paper [see above]

Vertically Integrated Projects: Secure Hardware | Atlanta, GA *January 2017 – December 2019*
Undergraduate Research Assistant, Team Lead
Project Title: Assessing the security potential of Non-Linear Multiple Input Signature Register (NLMISR)

- Researching (NLMISR) as alternative to Secure Hash Algorithm-2 (SHA-2) for low power/low area data encryption applications
- Designed 128-bit NLMISR and testing infrastructure (in VHDL) to search for hash collisions (empirical evaluation of collision resistance and other cryptographic properties)
- Team Lead (August 2017 – August 2018), Project Supervisor (August 2018 – December 2018)

Institute for Electronics and Nanotechnology, Georgia Tech | Atlanta, GA *May 2018 – August 2018*
Undergraduate Research Intern
Project Title: COSMOS: COmputational Skins for Multi-functional Objects and Systems
- Simulated novel MOSFET geometries and determined IV characteristics
- Designed and simulated circuits in Verilog-Analog using generated IV characteristics to assess transistor performance

National Science Foundation, Tennessee Technological University | Cookeville, TN *June 2017 – August 2017*
Undergraduate Research Intern
Project Title: Investigating Trojan Detection Mechanisms in a Modified AMBA
- Designed hardware Trojans to evaluated detection-avoidance capabilities using Fmax, area usage, power usage, signal analysis
- Determined that Trojans generally avoided detection successfully, performing within 15% of uninfected design in most criteria

Senior Project

ECE Senior Design | Atlanta, GA *August 2019 – May 2020*
- Developed communications protocol and analog interface circuit designs for **underwater acoustic modem**
- Analyzed underwater transmission models to develop TX and RX circuit amplifiers that interfaced with an acoustic transducer
- Selected ICs for circuit design, performed PCB layout, and conducted full TX-RX pipeline simulation in LTSpice
  - TX circuit amplified FPGA DAC signals via class-D amplifier with a 50V boost-converter output as the power supply; this configuration fed the amplified DAC signals to the transducer; RX circuit used 2-stage inverting bandpass filter
- Circuit fabrication and integration with FPGA (for full demonstration) was not feasible due to COVID-19 pandemic

Selected Coursework (R = Research, U = Undergrad, G = Grad)

Information Processing Models in Neural Systems (G): Mathematical models of neural activity, neural image processing and statistics
Computer Architecture (U, G): Multi-cycle machines; scalar/superscalar pipelining; memory systems & caching
Signal Processing (U): classical DSP (discrete and continuous time), Filter Design, DSP-centric probability/statistics, intro to information theory, dimensionality reduction
Hardware Security (R, U/G): Applied cryptography, crypto-VLSI design, physically unclonable functions, hardware design of secure roots of trust, operating systems/compiler fundamentals
Communication Systems (R): Automatic Modulation Classification using Machine Learning
Machine Learning for Trading (U/G): ML for Quantitative Finance
Other courses (U): Embedded Control Design, Analog Electronics, Computer Vision, Intro to AI, Intro to Computational Linguistics, Linear Algebra (MIT OpenCourseWare)

Skills

Programming: C, Python, MATLAB, Standard Meta Language, VHDL/Verilog, Assembly, Java
Software: Xilinx Vivado, LTSpice, Multisim, ModelSim, Altera Quartus
Hardware: FPGAs, microcontrollers, oscilloscopes, logic analyzers, bench-level test equipment
Communication: Research papers, technical presentations, technical documentation / instruction manuals
Languages: Hindi (fluent), Spanish (conversational), English (native), Marathi (native)

Activities

Intramurals Official | Atlanta, Georgia *August 2018 – May 2020*
Official for Campus Recreation Center
- Officiate flag football, basketball, soccer, softball
- Received Official of the Week honors (October 2019)

Vertically Integrated Projects | Atlanta, Georgia *June 2018 – May 2020*
VIP Ambassador
- Assist with outreach efforts to Georgia Tech students through information sessions and poster fairs to present current research efforts of various VIP teams
- Delivered presentation about overall VIP program efforts to Georgia Tech Admissions department for outreach efforts to incoming high-school students