Tarun Maddali

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Objective

Determined, disciplined, and diligent Masters' student with previous industry experience keen on internship opportunities in computer architecture and digital VLSI design that will allow me to utilize my skills in electronic device development and circuit design.

Education

University of Michigan | Ann Arbor, MI *August 2022 – Present*
Master of Science in Electrical and Computer Engineering, GPA: 3.2 Expected Graduation, April 2024
Integrated Circuits & VLSI Specialization

Georgia Institute of Technology | Atlanta, GA *August 2016 – May 2021*
Bachelor of Science in Electrical Engineering, GPA: 3.74 (Highest Honors)
Minor in Computing and Systems & Architecture

Skills

Programming: C, C++, Verilog, Assembly, VHDL, Java, Python, MATLAB, JavaScript, Tcl
Platforms: Ubuntu, Robot Operating System
Hardware: Raspberry Pi, ARM Mbed Microcontroller, FPGAs, Oscilloscope, Function Generator, Logic Analyzer, Power Supply, Multimeter, Arduino Microcontroller
Software: Altera Quartus II, NI LabVIEW, SolidWorks, GitHub, Eagle, Cadence, Multisim, ModelSim, Simulink, Shell Scripting, Innovus, Automatic Place & Route, Design Compiler, Silvaco, Synopsys Sentaurus TCAD, CUDA, Verdi
Equipment: Plasma Cutter, Laser Cutter, 3D Printer, PCB Laser/Plotter
Communication: Technical reports, Presentations

Projects

EECS 427 RISC Processor Project | University of Michigan *August 2022 – December 2022*
Team Member / EECS 427
EECS 427, otherwise known as VLSI Design 1, is a class that is focused on understanding topics from logical effort to dynamic logic gates. The end goal of the class is to design a RISC processor with a custom implementation of our choice.

- Utilized tools such as Cadence and Design Compiler to design different portions of the RISC processor such as the ALU and the Program Counter.
- Verified each section of the Processor, along with the entire processor operation, using NC – Verilog and understanding the resulting waveform outputs.
- Implemented a customization to the processor that implements a MAC (multiply and accumulate operation) with a custom SRAM cell to get the weights for the operation and an adder tree to perform the necessary computations.

Rogues Gallery Vertically Integrated Project Team| Georgia Tech *August 2019 – April 2021*
Team Member / Reconfigurable Computing Team
The Vertically Integrated Project Teams are focused on bringing in students from different disciplines to work with faculty on a multidisciplinary, multi-semester research project. The Rogues Gallery VIP Team is focused on creating and interface between new computer hardware and software techniques to solve future research and industry questions on computing.

- Explored different methods of using Field Programmable Gate Arrays in different application such as branch prediction and cryptography. The team contrived an idea to use cryptography and non-history branch prediction to make a more secure and efficient pipeline.
- Communicated with faculty advisor and other team members focused on project progression and development, which will result in a successful project presentation in front of faculty advisors, students, and members of the VIP Executive Team.
- Utilized tools such as PyRTL and Chisel to implement pipelined architecture, along with additional implementations specific to the project

Experience

Accenture | San Jose, CA *May 2021 – July 2022*

Software Architect Analyst (Firmware Engineering) / Silicon Design Service

Accenture is a services company that helps clients from across the world with their projects. The Silicon Design Service is a new section of the company that focuses on services for employers hoping to make improvements in the embedded landscape.

- Acted on a multitude of tasks related to products for a technology client in the realm of embedded systems and firmware engineering, specifically in the testing of these products, to improve that company's products.
- Utilized different programming languages such as C++ and Python and tools such as Shell Scripting to complete these tasks. These projects ranged from regression testing to virtual modeling.
- Collaborated with team members daily about each one's tasks and issues that may arise with these tasks.

Opportunity Research Scholars| Atlanta, GA **August 2019 – April 2021**

The ORS Program is an innovative program designed to help students network with faculty and industry sponsors and immerse in a collaborative project that is designed to enhance the academic experience of undergraduate students.

Undergraduate Research Assistant / Nanoelectronics Research Lab *August 2020 – April 2021*

- Explored new topics in algorithms and optimization in relation to computing systems, which resulted in a project focused on cache optimization using genetic algorithms in C and Verilog.
- Collaborated with four team members on an ECE research project, which resulted in a successful poster presentation in front of numerous faculty and students affiliated with the School of Electrical and Computer Engineering.
- Researched under the supervision of a graduate student to determine the weekly tasks and forward progress on the project. The graduate student's advice led to both a successful presentation and project, which was presented at the IEEE RFID Conference.

Undergraduate Research Assistant / Laboratory for Emerging Devices and Circuits *August 2019 – April 2020*

- Explored new topics in VLSI and hardware design, which resulted in a project focused on creating a PCB implementation of a neural network using a resistive-capacitive network.
- Collaborated with three team members on an ECE research project, which resulted in a successful poster presentation in front of numerous faculty and students affiliated with the School of Electrical and Computer Engineering.
- Researched under the supervision of a graduate student to determine the weekly tasks and forward progress on the project. The graduate student's advice led to both a successful presentation and project.

Relevant Coursework

EECS 470 – Computer Architecture (Winter 2023): Understanding how computer processors are implemented and how they can be optimized, which will lead to a final project involving a processor implementation in Verilog.

EECS 471 – Applied Parallel Programming with GPUs (Winter 2023): Investigating parallel computing applications and algorithms, and implementations, which will lead to a final project dealing with optimizations of a current problem

EECS 523 - Digital Integrated Technology: Learned about the technology behind digital chip design along with new technologies that will be important in the future of digital VLSI technology, all of which will culminate into a final project on looking into a specific device structure and applying certain effects to the specific device by changing its parameters.

EECS 427 - VLSI Design 1: Utilized CMOS technology and digital design/verification techniques to create different logic circuit designs, all of which eventually leads to a final project of a RISC processor with an added customization

VLSI and Advanced Digital Design (undergraduate course): Learned about different methods of implementing complex logical functions, utilized Cadence to design the cells for these functions

Introduction to Electronic Systems Packaging (undergraduate course): Learned about the design and optimization of computer hardware in terms of concepts such as interconnects

Cryptographic Hardware for Embedded Systems (undergraduate course): Understood different encryption standards, along with designing hardware for different cybersecurity applications

Advanced VLSI Systems (undergraduate course): Applied previous VLSI knowledge to more complex topics such as clocking, sequential elements, and memory

Digital Design Laboratory (undergraduate course): Analysis and testing of state machine circuit implementations using oscilloscope, design of controllers for a train simulation and a robot

Processor Design (undergraduate course): Implemented 5 different projects, all of which involved utilizing Verilog to create a pipelined architecture. By the end of the class, a pipeline with interrupt support was created and tested on an FPGA board.

Data Structures and Algorithms (undergraduate course): Understood concepts such as Binary Search Trees, Graphs, and Sorting Algorithms, and implemented these concepts using Java