Curriculum Vitae
John Kustin

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ACADEMIC BACKGROUND

Electrical Engineering Ph.D Candidate — Aug 2022 - Aug 2027
University of Michigan, Ann Arbor, MI
- Advised by Professor Michael P. Flynn

B.S. Electrical Engineering — Sept 2018 - June 2022
Stanford University, Stanford, CA
- GPA: 3.93/4.0
- Advised by Assistant Professor Priyanka Raina

PROJECTS

- **Bandgap Reference Circuit (2021)** - taped out in Skywater 130nm. Measured 1 sample. Specifications include 960 mV output with 125 ppm/°C using 60.5 μW at 1.8 V and occupying 0.0320 mm^2.
- **Modular FPGA and Programmable SoC Environment for ASIC Verification and Evaluation (2020)** - cosimulate software apps with RTL and then deploy a verification and evaluation environment to an FPGA.

WORK EXPERIENCE

High Speed AMS Circuit Design Intern — June 2022 - August 2022
Apple Inc., Cupertino, California
- PLL team.

Hardware Technology Intern — June 2021 - September 2021
Apple Inc., Cupertino, California
- Analog/Mixed Signal team.
- Automation and Methodology.

Undergraduate Researcher — March 2020 - November 2020
Robust Systems Group, Stanford, California
- Created and used a measurement platform to study SoC power and latency.
- Wrote Python to coordinate I^{2}C and GPIO enabled power measurement for SoCs.
- Used Petalinux to create an environment for rapid co-simulation of FPGA and ARM CPU on ZC706.

Applications Engineer Intern — June 2019 - September 2019
Analog Devices Inc., San Jose, California
- Wrote a C library to enable the ADALM2000 portable lab to function as a high-speed, large buffered data acquisition unit for capacitive sensing applications.

LITERATURE

- **CHIMERA: A 0.92 TOPS, 2.2 TOPS/W Edge AI Accelerator with 2 MByte On-Chip Foundry Resistive RAM for Efficient Training and Inference**
  Kartik Prabhu, Albert Gural, Zainab F. Khan, Robert M. Radway, Massimo Giordano, Kalhan Koul, Rohan Doshi, **J. W. Kustin**, Timothy Liu, Gregorio B. Lopes, Victor Turbiner, Win-San Khwa, Yu-Der Chih, Meng-Fan Chang, Guenole Lallement, Boris Murmann, Subhasish Mitra, Priyanka Raina

Journal of Solid-State Circuits, vol. 57, no. 4, pp. 1013-1026, April 2022, doi: 10.1109/JSSC.2022.3140753. Paper

- **CHIMERA: A 0.92 TOPS, 2.2 TOPS/W Edge AI Accelerator with 2 MByte On-Chip Foundry Resistive RAM for Efficient Training and Inference**
  M. Giordano, K. Prabhu, K. Koul, R. M. Radway, A. Gural, R. Doshi, Z. F. Khan, **J. W. Kustin**, T. Liu, G. B. Lopes, V. Turbiner, W.-S. Khwa, Y.-D. Chih, M.-F. Chang, G. Lallement, B. Murmann, S. Mitra, P. Raina
  2021 Symposium on VLSI Circuits, 2021, pp. 1-2, doi: 10.23919/VLSICircuits52068.2021.9492347. Paper

AWARDS

- Stanford University Department of Electrical Engineering Student Design Project Award. June 2022. Related work: Bandgap circuit.

TEACHING ASSISTANT

- Introduction to VLSI Systems (EE 271). Fall 2021.
- Lab64 makerspace. Sept 2019 to July 2020.